What is claimed is:

1. A multiplexer circuit comprising:

a first tri-state inverter circuit that is coupled to a first multiplexer input node, a first multiplexer output node, and a first switch node, wherein

the first tri-state inverter circuit is capable of a high-impedance output at the first multiplexer output node;

a second tri-state inverter circuit that is coupled to a second multiplexer input node, a second multiplexer output node, and a second switch node, wherein

the second tri-state inverter circuit is capable of a high-impedance output at the second multiplexer output node;

a first switch circuit that is coupled between the first switch node and the second multiplexer output node; and

a second switch circuit that is coupled between the second switch node and the first multiplexer output node.

2. The multiplexer circuit of Claim 1, wherein

the first tri-state inverter circuit is configured to isolate the first multiplexer input node from the first multiplexer output node if a control signal corresponds to a second logic level.

3. The multiplexer circuit of Claim 2, wherein

the second tri-state inverter circuit is configured to isolate the second multiplexer input node from the second multiplexer output node if a control signal corresponds to the second logic level,

the first switch circuit is configured to:

short the first switch node to the second output node if the control signal corresponds to a second logic level, and

isolate the first switch node from the second output node if the control signal corresponds to a first logic level, and

the second switch circuit is configured to:

short the second switch node to the first multiplexer output node if the control signal corresponds to the second logic level, and

isolate the second switch node from the first multiplexer output node if the control signal corresponds to the first logic level.

4. The multiplexer circuit of Claim 2, wherein

the first tri-state inverter circuit is further configured:

to provide an inverter output signal at the first multiplexer output node in response to a first multiplexer input signal if the control signal corresponds to a first logic level, and

provide the inverter output signal at the first switch node in response to the first multiplexer input signal.

5. The multiplexer circuit of Claim 1, further comprising:

a third switch circuit that is coupled between the first multiplexer output node and a third switch node;

a fourth switch circuit that is coupled between the second multiplexer output node and a fourth switch node;

a high-range decoder circuit that is coupled to the third switch node; and

a low-range decoder circuit that is coupled to the fourth switch node.

6. The multiplexer circuit of Claim 5, wherein the third switch circuit comprises a first transmission gate, and the fourth switch circuit comprises a second transmission gate.

7. The multiplexer circuit of Claim 1, wherein:

the first tri-state inverter circuit is configured to:

receive a first multiplexer input signal at the first multiplexer input node,

receive a first control signal,

receive a complement of the first control signal,

provide a first inverter signal at the first switch node and a fifth switch node in response to the first multiplexer input signal, and

provide the first inverter signal at the first multiplexer output node in response to the first multiplexer input signal if the first control signal corresponds to a first logic level, and

the second tri-state inverter circuit is configured to:

receive a second multiplexer input signal at the second multiplexer input node,

receive the first control signal,

receive a complement of the first control signal,

provide a second inverter signal at the second switch node and a sixth switch node in response to the second multiplexer input signal, and

provide the second inverter signal at the second multiplexer output node in response to the second multiplexer input signal if the second control signal corresponds to the first logic level.

8. The multiplexer circuit of Claim 7, wherein

the first switch circuit is further coupled to the fifth switch node,

the first switch circuit is configured to:

receive the first control signal and the complement of the first control signal, and

provide the first inverter signal at the second multiplexer output node if the first control signal corresponds to a second logic level,

the second switch circuit is further coupled to the sixth switch node, and

the second switch circuit is configured to:

receive the first control signal and the complement of the first control signal, and

provide the second inverter signal at the first multiplexer output node if the first control signal corresponds to the second logic level.

9. The multiplexer circuit of Claim 1, wherein

the multiplexer circuit consists of twelve transistors,

the first tri-state inverter circuit is configured to receive a first multiplexer input signal,

the multiplexer circuit is arranged such that the first multiplexer input signal drives at most two transistors of the twelve transistors,

the second tri-state inverter circuit is configured to receive a second multiplexer input signal, and

the multiplexer circuit is arranged such that the second multiplexer input signal drives at most another two transistors of the twelve transistors.

10. The multiplexer circuit of Claim 1, wherein

the first tri-state inverter circuit comprises:

a first p-type transistor having:

a gate that is coupled to the first multiplexer input node,

a drain that is coupled to the first switch node, and

a source that is coupled to a first power supply node,

a second p-type transistor having:

a gate that is coupled to a first control node,

a drain that is coupled to the first multiplexer output node, and

a source that is coupled to the first switch node,

a first n-type transistor having:

a gate that is coupled to a second control node;

a drain that is coupled to the first multiplexer output node, and

a source that is coupled to the fifth switch node, and

a second n-type transistor having:

a gate that is coupled to the first multiplexer input node,

a drain that is coupled to a fifth switch node, and

a source that is coupled to a second power supply node, and

the first switch circuit comprises:

a third p-type transistor comprising:

a gate that is coupled to the second control node,

a drain that is coupled to the second multiplexer output node, and

a source that is coupled to the first switch node, and

a third n-type transistor comprising:

a gate that is coupled to the first control node,

a drain that is coupled to the second multiplexer output node, and

a source that is coupled to the fifth switch node.

11. A multiplexing column driver circuit comprising:

a plurality of channels arranged in pairs, wherein a selected pair of the pairs comprises a first two-by-two multiplexer circuit, wherein the first two-by-two multiplexer circuit comprises:

a first tri-state inverter circuit that is coupled to a first multiplexer input node, a first multiplexer output node, and a first switch node;

a second tri-state inverter circuit that is coupled to a second multiplexer input node, a second multiplexer output node, and a second switch node;

a first switch circuit that is coupled between the first switch node and the second multiplexer output node; and

a second switch circuit that is coupled between the second switch node and the first multiplexer output node.

12. The multiplexing column driver circuit of Claim 11, wherein

one of the channels of the selected pair further comprises:

a first transmission gate that is coupled between a first channel input node and a first latch node,

a first latch circuit that is coupled between the first latch node and the first multiplexer input node,

a second transmission gate that is coupled between the first multiplexer output node and a second latch node, and

a second latch circuit that is coupled between the second latch node and a first inverter node.

13. The multiplexing column driver circuit of Claim 11, wherein

the selected pair further comprises:

a high-range decoder circuit that is coupled between a first decoder node and a third multiplexer input node; and

a low-range decoder circuit that is coupled between a second decoder node and a fourth multiplexer input node.

14. The multiplexing column driver circuit of Claim 13, wherein

the selected pair further comprises:

a second two-by-two multiplexer circuit that is coupled to the third multiplexer input node, the fourth multiplexer input node, a third multiplexer output node, and a fourth multiplexer output node.

15. The multiplexing column driver circuit of Claim 11, wherein

the first tri-state inverter circuit is configured to isolate the first multiplexer input node from the first multiplexer output node if a control signal corresponds to a second logic level.

16. The multiplexing column driver circuit of Claim 14, wherein

the second tri-state inverter circuit is configured to isolate the second multiplexer input node from the second multiplexer output node if a control signal corresponds to the second logic level,

the first switch circuit is configured to:

short the first switch node to the second output node if the control signal corresponds to the second logic level; and

isolate the first switch node from the second output node if the control signal corresponds to a first logic level; and

the second switch circuit is configured to:

short the second switch node to the first multiplexer output node if the control signal corresponds to the second logic level; and

isolate the second switch node from the first multiplexer output node if the control signal corresponds to the first logic level.

17. The multiplexing column driver circuit of Claim 11, wherein

the first tri-state inverter circuit is further configured:

to provide an inverter output signal at the first multiplexer output node in response to a first multiplexer input signal if the control signal corresponds to a first logic level, and

provide the inverter output signal at the first switch node in response to the first multiplexer input signal.

18. The multiplexing column driver circuit of Claim 11, wherein

the first two-by-two multiplexer circuit consists of twelve transistors;

the first tri-state inverter circuit is configured to receive a first multiplexer input signal;

the second tri-state inverter circuit is configured to receive a second multiplexer input signal; and

the first two-by-two multiplexer circuit is arranged such that

the first multiplexer input signal drives at most two transistors of the twelve transistors, and

the second multiplexer input signal drives at most another two transistors of the twelve transistors.

19. The multiplexing column driver circuit of Claim 11, wherein

the first tri-state inverter circuit is configured to:

receive a first multiplexer input signal at the first multiplexer input node;

receive a first control signal;

receive a complement of the first control signal;

provide a first inverter signal at the first switch node and a fifth switch node in response to the first multiplexer input signal; and

provide the first inverter signal at the first multiplexer output node in response to the first multiplexer input signal if the first control signal corresponds to a first logic level;

the second tri-state inverter circuit is configured to:

receive a second multiplexer input signal at the second multiplexer input node;

receive the first control signal;

receive a complement of the first control signal;

provide a second inverter signal at the second switch node and a sixth switch node in response to the second multiplexer input signal; and

provide the second inverter signal at the second multiplexer output node in response to the second multiplexer input signal if the second control signal corresponds to the first logic level;

the first switch circuit is further coupled to the fifth switch node;

the first switch circuit is configured to:

receive the first control signal and the complement of the first control signal; and

provide the first inverter signal at the second multiplexer output node if the first control signal corresponds to a second logic level;

the second switch circuit is further coupled to the sixth switch node; and

the second switch circuit is configured to:

receive the first control signal and the complement of the first control signal; and

provide the second inverter signal at the first multiplexer output node if the first control signal corresponds to the second logic level.

20. A multiplexer circuit comprising:

a first means for providing a first inverted signal at a first multiplexer output node in response to a first multiplexer input signal if a control signal corresponds to a first logic level, wherein

the first means for providing is capable of a high-impedance output at the first multiplexer output node;

a second means for providing a second inverted signal at a second multiplexer output node in response to a second multiplexer input signal if the control signal corresponds to the first logic level, wherein

the second means for providing is capable of a high-impedance output at the second multiplexer output node; and

a means for coupling the first inverted signal from a first switch node to the second multiplexer output node if the control signal corresponds to a second logic level.